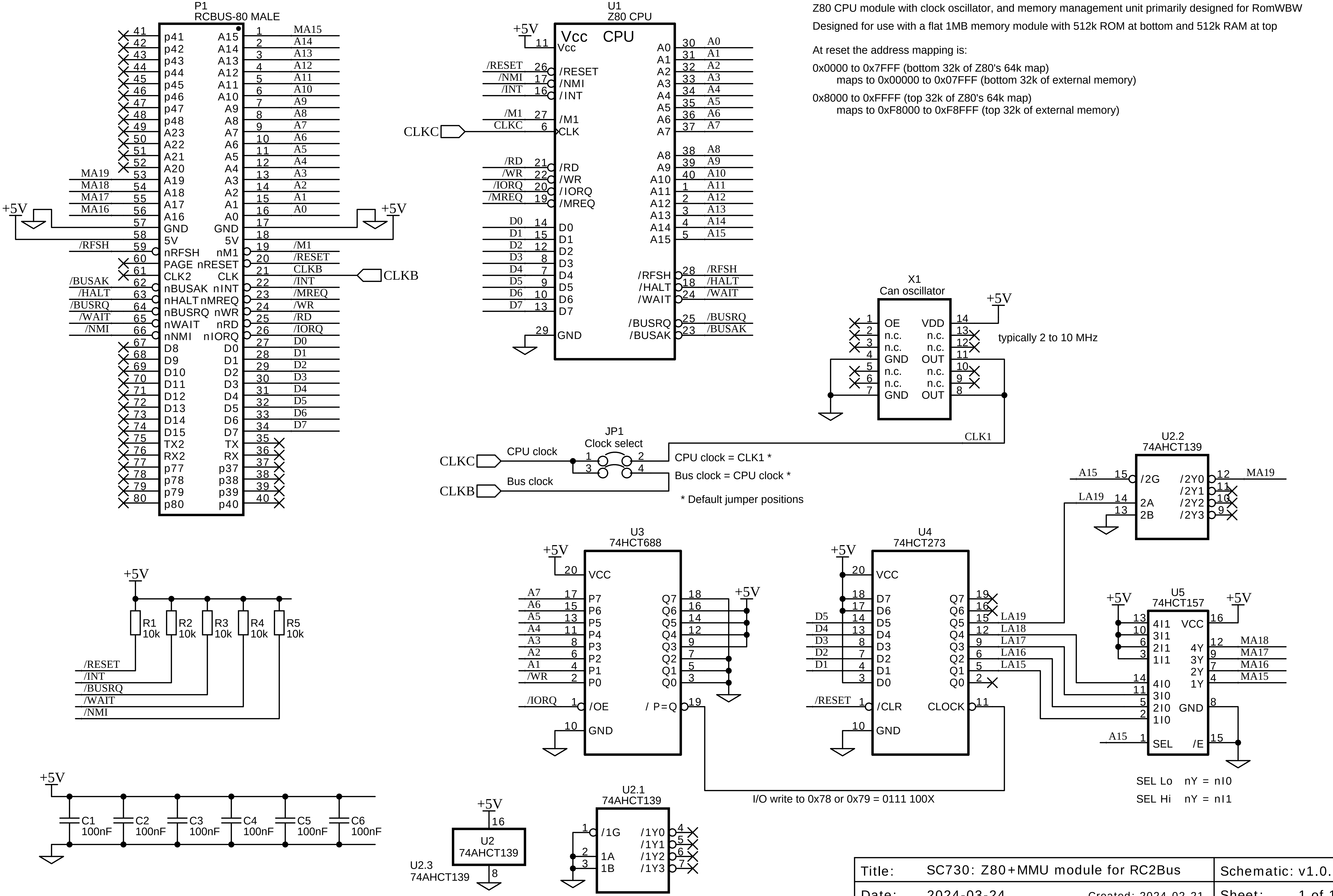

Z80 CPU module with clock oscillator, and memory management unit primarily designed for RomWBW

Designed for use with a flat 1MB memory module with 512k ROM at bottom and 512k RAM at top

At reset the address mapping is:

0x0000 to 0x7FFF (bottom 32k of Z80's 64k map)
maps to 0x00000 to 0x07FFF (bottom 32k of external memory)

0x8000 to 0xFFFF (top 32k of Z80's 64k map)
maps to 0xF8000 to 0xF8FFF (top 32k of external memory)

Title:	SC730: Z80+MMU module for RC2Bus	Schematic: v1.0.0
Date:	2024-03-24 Created: 2024-02-21	Sheet: 1 of 1
Designer:	Stephen C Cousins, Small Computer Central, www.scc.me.uk	