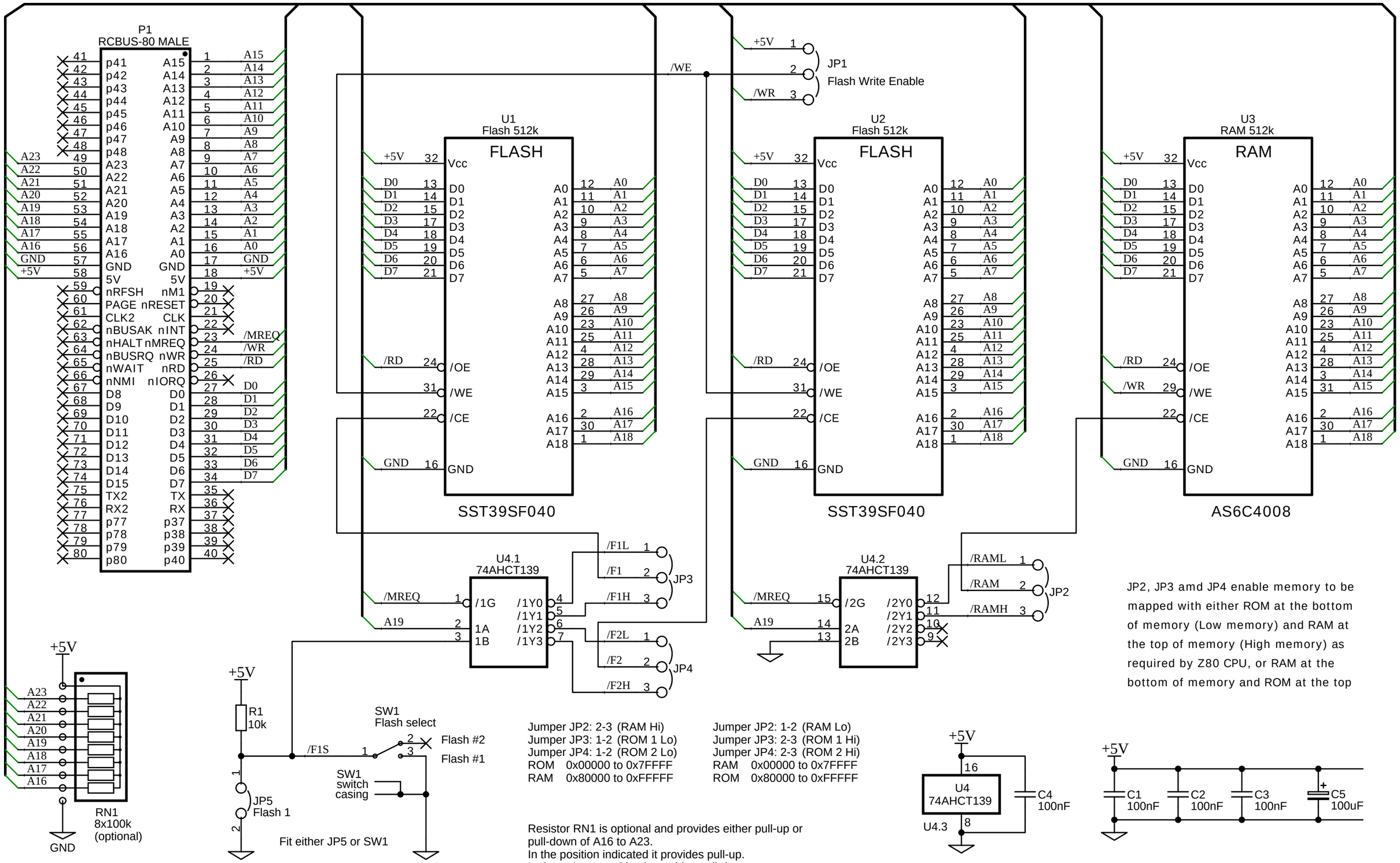

JP2, JP3 amd JP4 enable memory to be mapped with either ROM at the bottom of memory (Low memory) and RAM at the top of memory (High memory) as required by Z80 CPU, or RAM at the bottom of memory and ROM at the top

Jumper JP2: 2-3 (RAM Hi)
Jumper JP3: 1-2 (ROM 1 Lo)
Jumper JP4: 1-2 (ROM 2 Lo)
ROM 0x00000 to 0x7FFFF
RAM 0x80000 to 0xFFFFF

Jumper JP2: 1-2 (RAM Lo)
Jumper JP3: 2-3 (ROM 1 Hi)
Jumper JP4: 2-3 (ROM 2 Hi)
RAM 0x00000 to 0x7FFFF
ROM 0x80000 to 0xFFFFF

Resistor RN1 is optional and provides either pull-up or pull-down of A16 to A23.
In the position indicated it provides pull-up.
In the reverse position it provides pull-down.

Memory module with 512kB RAM and two 512kB Flash ROM arranged as a single flat 1MB bank of 512k ROM and 512k RAM
An 8-bit processor with a 16-bit address bus will require a memory management to generate the required 20-bit address bus

Title:	SC721: Memory 512k RAM + 512k ROM	Schematic: v1.0.0
Date:	2023-08-08 Created: 2023-07-21	Sheet: 1 of 1
Designer:	Stephen C Cousins, Small Computer Central, www.scc.me.uk	