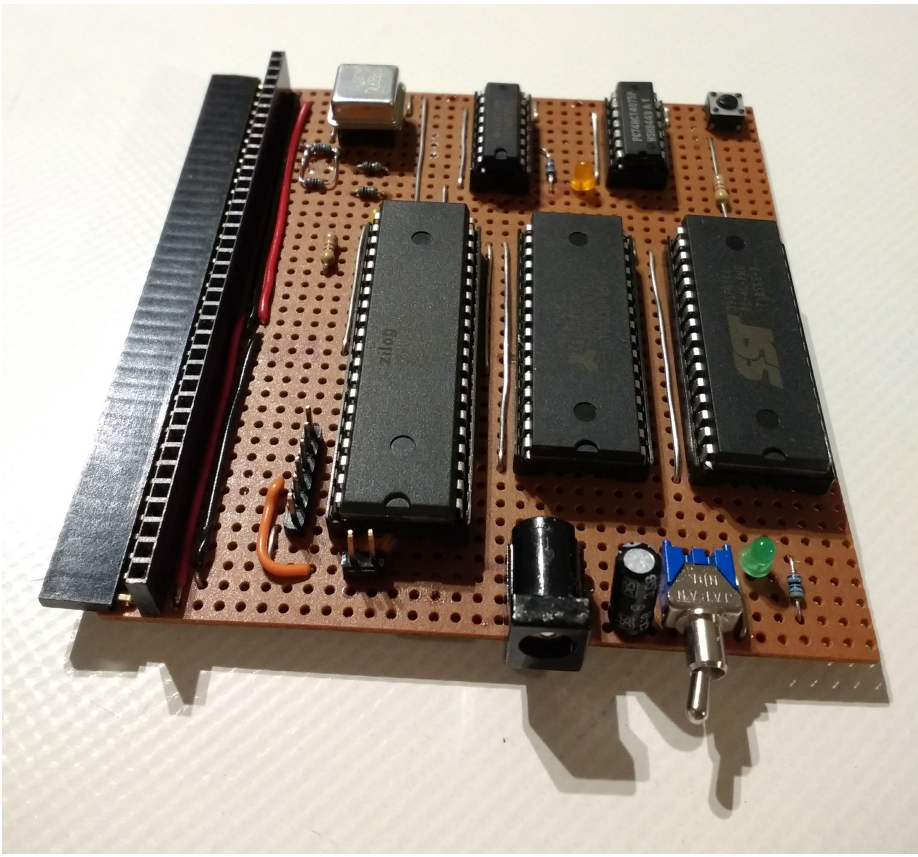
# Small Computer 101

# Circuit Description

**For Schematic 1.00**

Design and Documentation by Stephen C Cousins Document edition 1.0.0

# The Prototype



# Circuit Description

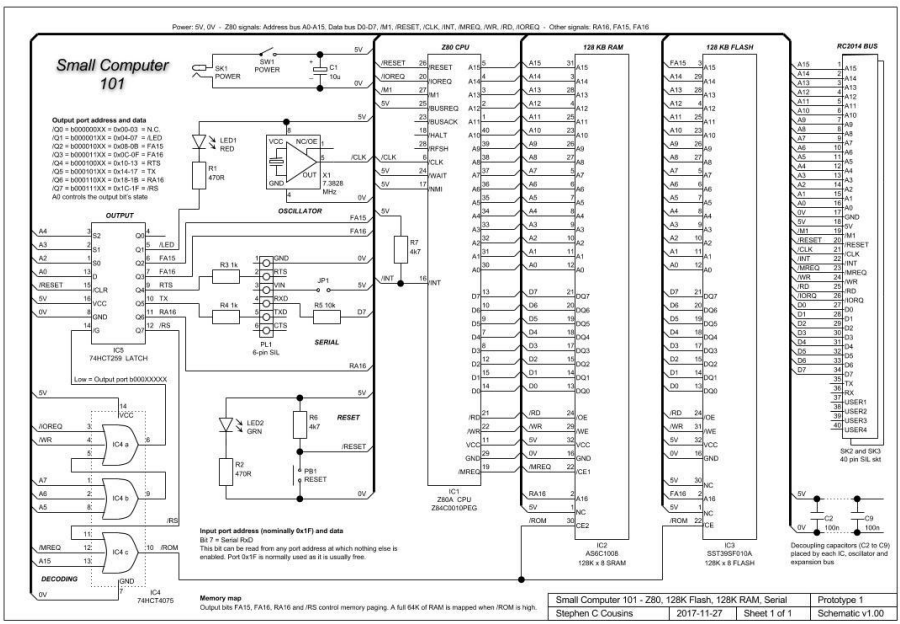
A prototype of the Small Computer 101 has been built and works as expected.

SC101 is a slightly cut down version of the paper design SC002.

The main features of the design are:

- Low cost, low component count, single board
- Z80 based with 128k bytes FLASH and 128k bytes RAM
- Bit-bang software serial port (115200 bits per second)
- Compatible with the Small Computer Monitor
- Expansion via RC2014 bus (2 sockets fitted)

Full schematic and parts list (with suppliers and price guide) are available as separate files.



## Memory

The SC101 supports 128k bytes of RAM plus 128k bytes of FLASH.

At reset the memory is mapped such that the bottom 32k bytes of the FLASH memory occupies the bottom 32k bytes of the memory map, with the top 32k bytes being RAM.

The FLASH memory can self modify itself to allow the firmware to be FLASHed or the space to be used for data storage. Not yet tested.

The output latch has four outputs to manage memory mapping:

Signals FA15 (FLASH address 15) and FA16 (FLASH address 16) provide selection of the currently accessible 32k byte bank of the 128k byte FLASH memory.

Signal /RS (ROM select, active low) can be raised to 5 volts to remove the FLASH from the memory map, leaving a full 64k bytes of RAM.

Signal RA16 (RAM address 16) can be raised to swap 64k RAM banks.

## Power

The SC101 can be powered from a USB socket or from the FTDI style serial cable.

The power socket (SK1) is a 2.1mm barrel style with centre positive. If the board is to always be powered by the FTDI cable, this component and power switch (SW1) could be left out.

LED2 is a power on indicator. This component and the associated resistor R2 are optional.

## Oscillator

The processor runs at 7.3728MHz. The clock is provided by a QX8T50B oscillator module.

This clock speed has been selected to match the standard RC2014 clock. Having selected this speed, it can not be changed without affecting the bit-band software serial port's bit rate.

## Decoding

IC4 (74HC4075) is a triple 3-input OR gate. This provides address decoding for IC5 (74HC259) which is an 8-bit addressable latch. It also generates the ROM enable / RAM disable signal.

## Output Latch

Output bits are provided by IC5 (74HC259), an 8-bit addressable latch. An addressable latch is used as individual bits can be controlled more easily than a traditional 8-bit D-type latch.

Each output is mapped to a 4 I/O address range. The data latched into the device is actually the address bus signal A0. Thus writing to even numbered I/O address clears the latch bit, while writing to an odd numbered I/O address sets the latch bit.

The Z80 instruction “OUT (<address>),A” can be used to set and clear output bits. The value of A Is irrelevant and the instruction does not affect any flags. So a single instruction can be used with no dependence on register values and no impact on the processor status flags.

Output Q1 controls LED1. If this LED is not required, the LED and the associated resistor (R1) can be left out without problems.

Output port address and data:

| | |
|---|---|
| /Q0 = Address b000000XX = 0x00-03 | No connection |
| /Q1 = Address b000001XX = 0x04-07 | LED on/off, active low (/LED1) |
| /Q2 = Address b000010XX = 0x08-0B | FLASH address 15 (FA15) |
| /Q3 = Address b000011XX = 0x0C-0F | FLASH Address 16 (FA16) |
| /Q4 = Address b000100XX = 0x10-13 | TTL level RTS |
| /Q5 = Address b000101XX = 0x14-17 | TTL level TxD |
| /Q6 = Address b000110XX = 0x18-1B | RAM address 16 (RA16) |
| /Q7 = Address b000111XX = 0x1C-1F | ROM select, active low (RA16) |

A0 controls the output bit’s state

## Input Data

There is only one input bit and this avoids an input buffer chip by feeding its signal to the data bus via a resistor. When inputs are read from a port address which has no active device, the data bus follows the input signal via the resistors.

A further 7 simple inputs could be added by this method is required.

If the bit-bang software serial port is not required, R5 can be left out and the bus will not be loaded.

## Serial Port

The serial port is a simple bit-bang software interface. It can run at 115200 bits per second. This has been tested as far as simple sending and receiving, but has yet to be integrated into the Small Computer Monitor ROM.

Some problems have been experienced by RC2014 users where the value of the RTS and TxD resistors have had to be lowered from the original 2k2 in order for some FTDI style cables to work. The resistors used here are 1k, which seems to be a compromise others have found satisfactory in most cases.

If the board is to be always powered from the FTDI cable, then these resistors can be replaced with direct connections. The resistors are there to limit current when the FTDI cable is powered but the SC101 board is not.

If this port is not required. R3, R4, R5 and PL1 can be left out.

## Expansion

Expansion is provided by RC2014 socket(s).

If expansion is not required the two RC2014 sockets can be left out. If so, interrupts will not be accessible, so R7 can be left out and the INT line tied to 5 volts.

The prototype have one vertical RC2014 connector and one horizontal connector. Having a choice during development is handy. This arrangement also takes up less space on the board than two vertical sockets. Also the horizontal socket allows a simple bus extender to be connected. This could be a very simple construction made from strip-board (Veroboard).

# Contact Information

If you wish to contact me regarding my Small Computer Designs please use the contact page at [www.scc.me.uk](http://www.scc.me.uk) (or smallcomputercentral.wordpress.com).

Issues related to the RC2014 can be posted on the RC2014-Z80 google grooup.

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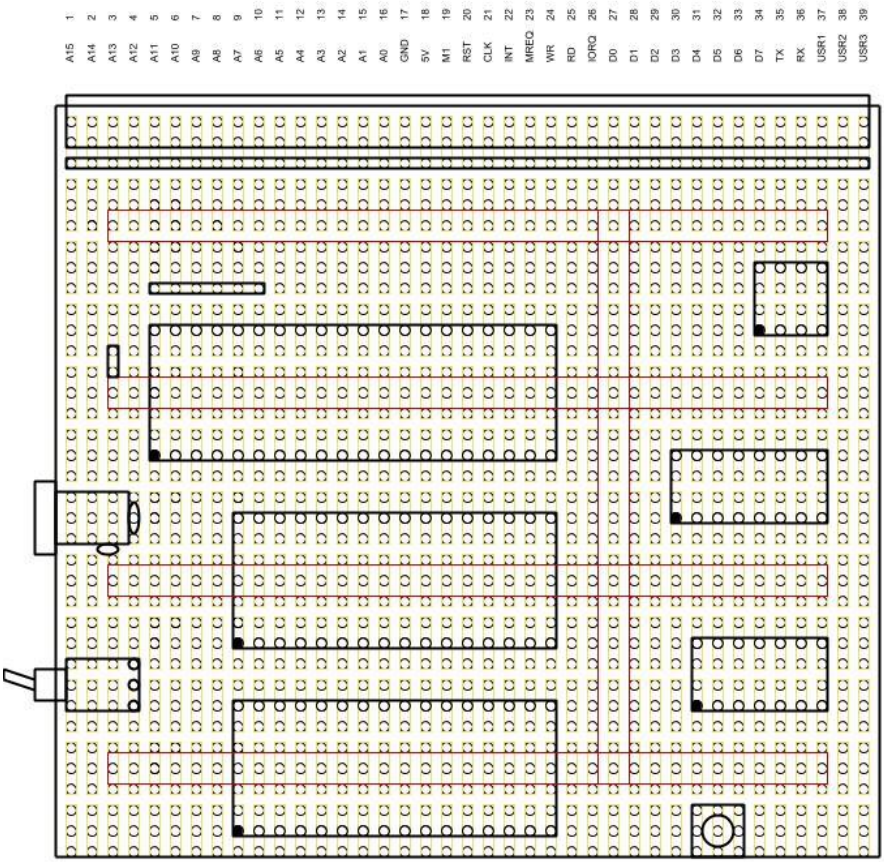

# Photo Gallery

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