Small Computer
002

Circuit Description

For Schematic 0.06

Design and Documentation by Stephen C Cousins Document edition 1.0.0

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Circuit Description

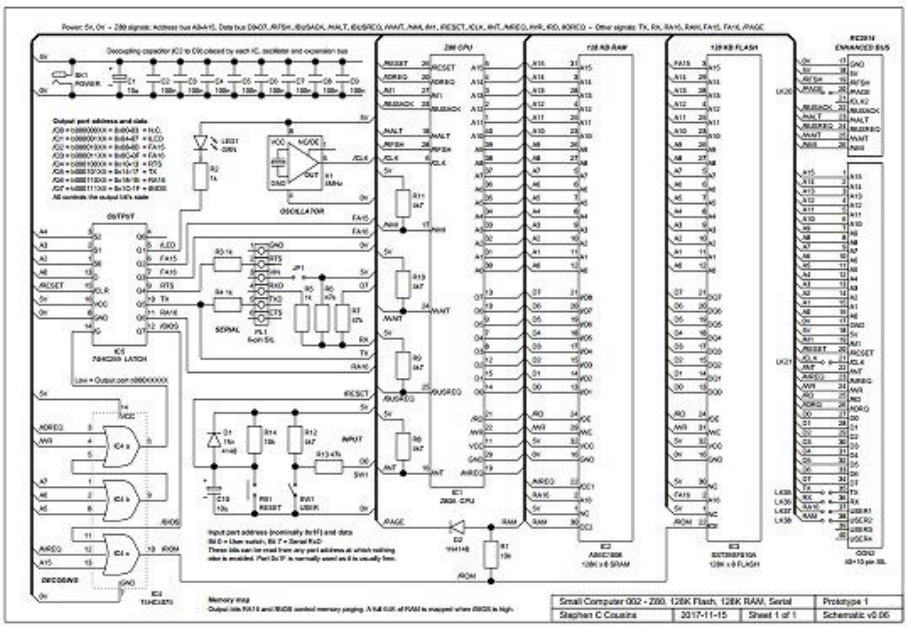
The Small Computer 002 is currently a paper design only and has not been built.

SC002 is a slightly enhanced version of SC001.

The main features of the design are;

- Low cost, low component count, single board
- Z80 based with 128k bytes FLASH and 128k bytes RAM
- Bit-bash serial port (115200 bits per second)
- Compatible with the Small Computer Monitor
- Expansion via RC2014 bus

Full schematic is available as a separate file.



Memory

The SC002 supports 128k bytes of RAM plus 128k bytes of FLASH.

At reset the memory is mapped such that the bottom 32k bytes of FLASH occupies the bottom 32k bytes, with the top 32k bytes being RAM.

The FLASH memory can self modify itself to allow the firmware to be FLASHed or the space to be used for data storage.

The output latch has two outputs to manage memory mapping:

Signals FA15 and FA16 provide selection of the currently accessible 32k byte bank of the 128k byte FLASH memory.

Signal /BIOS can be raised to 5 volts to remove the FLASH from the memory map, leaving a full 64k bytes of RAM.

Signal RA16 can be raised to swap 64k RAM banks.

Power

The SC002 can be powered from a USB socket or from the FTDI style serial cable.

The power socket is a 2.1mm barrel style with centre positive.

Oscillator

The processor runs as 4MHz. The clock is provided by a 5H8ET-4.000 oscillator module.

Decoding

IC4 (74HC4075) is triple 3-input OR gate. This provides address decoding for IC5 (74HC259) which is an 8-bit addressable latch. It also generates the RAM enable / ROM disable signal.

Output Latch

Output bits are provided by IC5 (74HC259), an 8-bit addressable latch. An addressable latch is used as individual bits can be controlled more easily than a traditional 8-bit D-type latch.

Each output is mapped to a 4 I/O address range. The data latched into the device is actually the address bus signal A0. Thus writing to even numbered I/O address clears the latch bit, while writing to an odd numbered I/O address sets the latch bit.

The Z80 instruction “OUT (<address>),A” can be used to set and clear output bits. The value of A Is irrelevant and the instruction does not affect any flags. So a single instruction can be used with no dependence on register values and no impact on the processor status flags.

Input Data

Inputs avoid an input buffer chip by feeding their signals to the data bus by resistors. When inputs are read from a port address which has no active device, the data bus follows the input signals via the resistors.

Expansion

Expansion is provided by RC2014 socket(s).

Contact Information

If you wish to contact me regarding my Small Computer Designs please use the contact page at www.scc.me.uk (or smallcomputercentral.wordpress.com).

Issues related to the RC2014 can be posted on the RC2014-Z80 google grooup.

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